

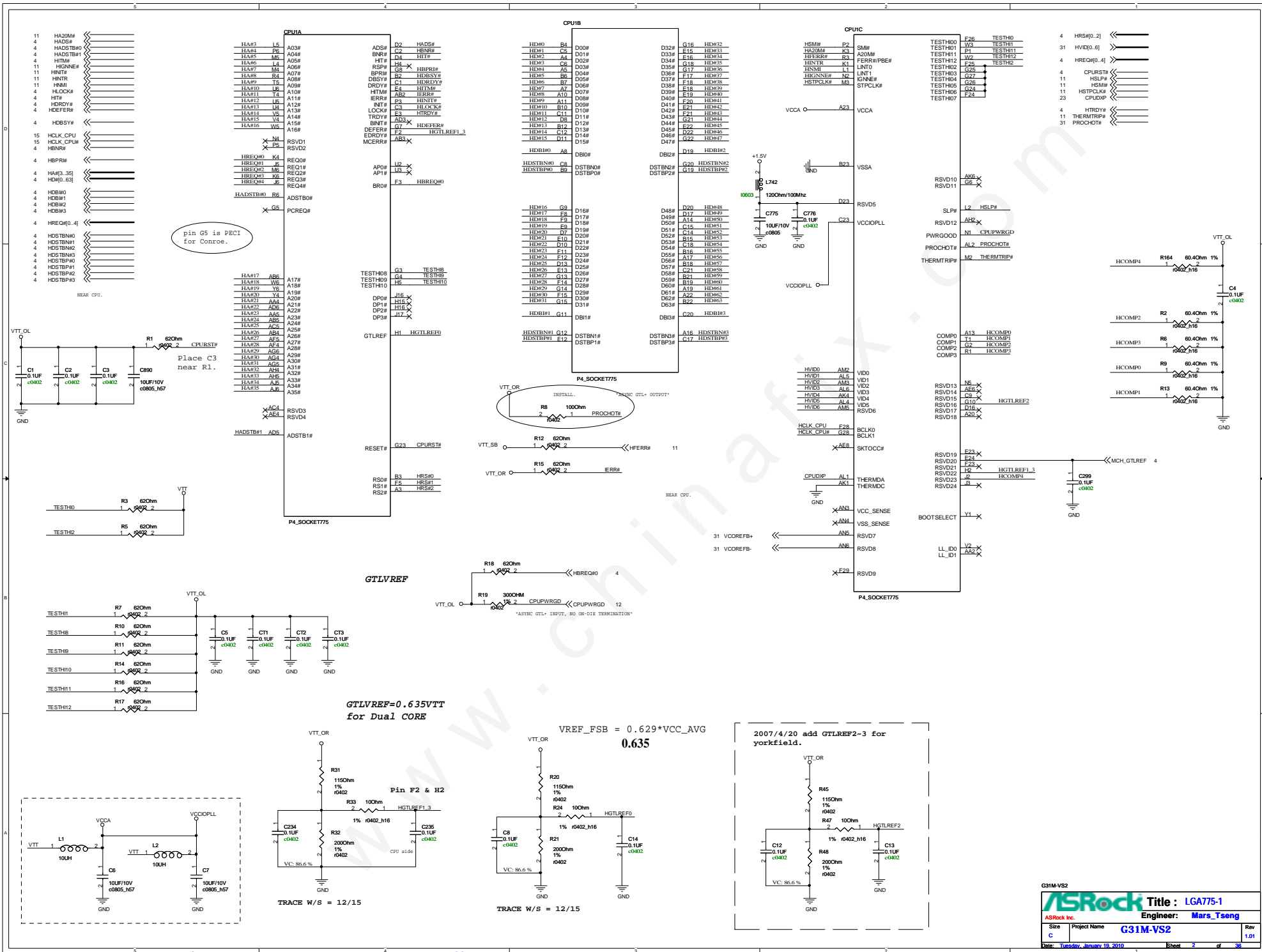
# Asrock INTEL G31M-VS Schematics

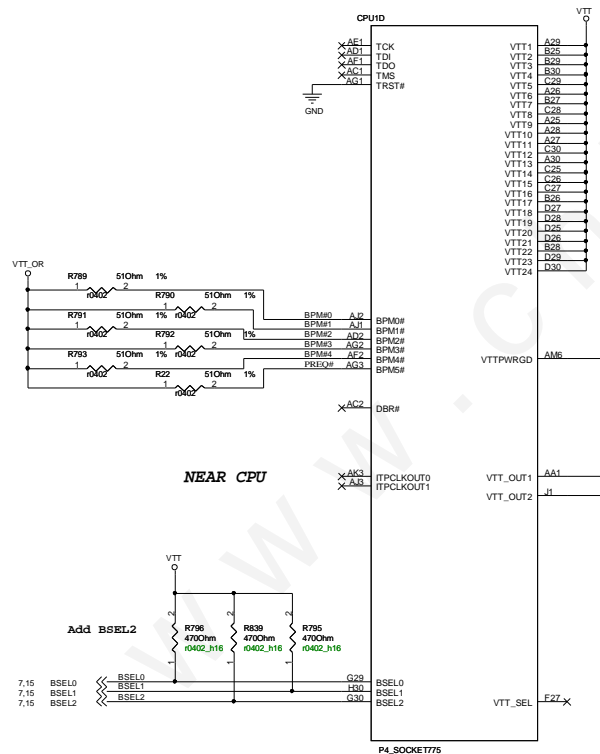
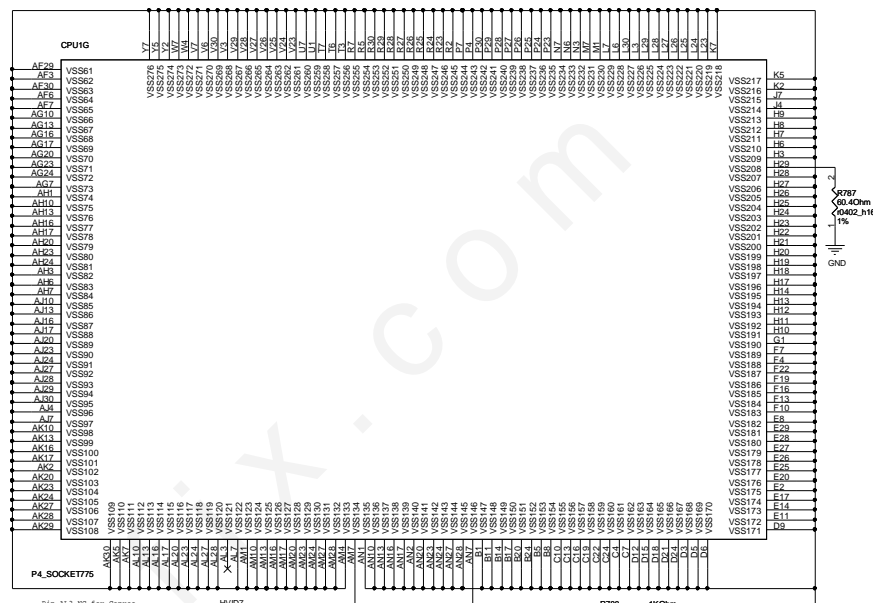
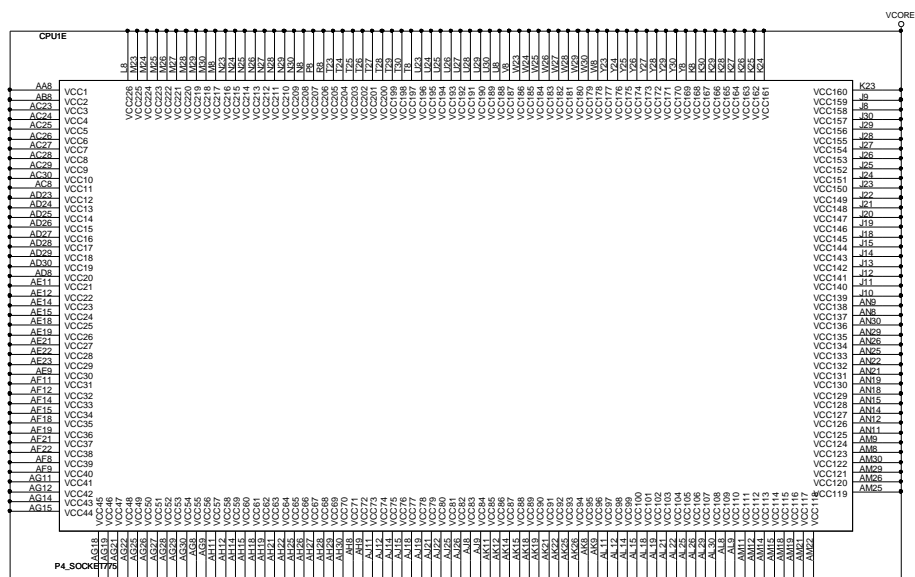
Revision G/A 1.01

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G31M-VS2

<b>ASRock</b>		<b>Title : COVER SHEET</b>	
ASRock Inc.		Engineer: Mars_Tseng	
Size Custom	Project Name <b>G31M-VS2</b>	Rev 1.01	
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CK409 BSEL TABLE:

BSEL0	BSEL1	BSEL2	FSB
0	0	0	100MHz
0	0	1	133MHz
0	1	0	200MHz
1	1	0	266MHz
1	1	1	333MHz
1	1	1	400MHz

(OD needs pull up to +3V)

CK410 BSEL TABLE:

BSEL0	BSEL1	BSEL2	FSB
1	0	1	100MHz
0	0	1	133MHz
0	1	0	200MHz
0	0	0	266MHz
1	0	0	333MHz
1	1	0	400MHz

(OD needs pull up to +3V)

"Support FSB 100/133/200 MHz"

"Support FSB 266/333/400 MHz"





```

>>> MD_A[3..0] 5
>>> MAA_A[14..0] 5
>>> MAB_A[2..0] 5
>>> MBDT_A[1..0] 5
>>> MDOB_A[7..0] 5
>>> MCKE_A[1..0] 5
>>> MCS_A0# 5
>>> MCS_A1# 5

>>> MWE_A# 5
>>> MCAS_A# 5
>>> MRAS_A# 5

>>> CK_DIMM_A0 5
>>> CK_DIMM_A0# 5
>>> CK_DIMM_A1 5
>>> CK_DIMM_A1# 5
>>> CK_DIMM_A2 5
>>> CK_DIMM_A2# 5

>>> MDQS_A7# 5
>>> MDQS_A7 5
>>> MDQS_A6# 5
>>> MDQS_A6 5
>>> MDQS_A5# 5
>>> MDQS_A5 5
>>> MDQS_A4# 5
>>> MDQS_A4 5
>>> MDQS_A3# 5
>>> MDQS_A3 5
>>> MDQS_A2# 5
>>> MDQS_A2 5
>>> MDQS_A1# 5
>>> MDQS_A1 5
>>> MDQS_A0# 5
>>> MDQS_A0 5

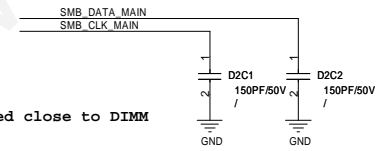
>>> SMB_CLK_MAIN 12,15,18
>>> SMB_DATA_MAIN 12,15,18

```

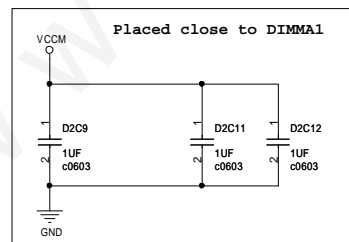
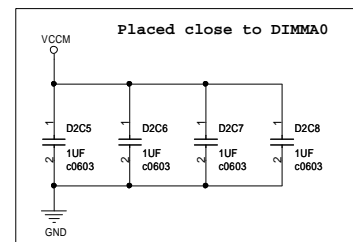
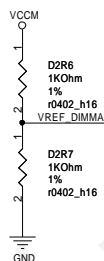
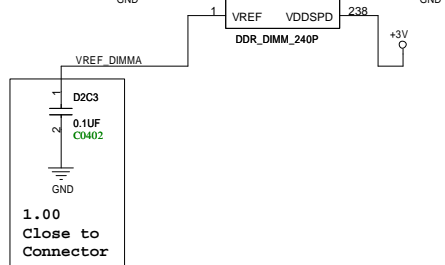
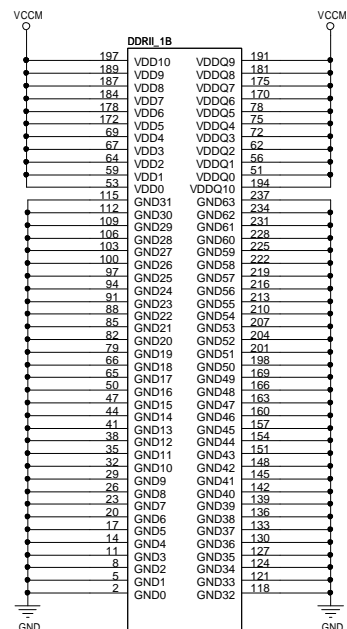
There status Off,75,150 Ohm

The schematic diagram illustrates the internal structure of a 1T1R1C1 DRAM cell. It features two vertical columns of components. The left column consists of an access transistor (SW1) at the top, followed by two resistors (Rval1 and Rval2) in series, and another access transistor (SW1) at the bottom. The right column is identical but uses SW2 and Rval2 resistors. Both columns are connected to a top supply rail (Vddq) and a bottom supply rail (Vssq). On the left, a 'DRAM input buffer' is connected to the top of the first access transistor (SW1). On the right, a 'DRAM DQ input pin' is connected to the top of the second access transistor (SW2).

- Controlled by memory controller via ODT pin.
- Can be turned on/off in 2 cycles
- Provides active termination at the receiver interface.



G31M-VS2		 <b>Title :</b> DDR2-CHA Control	
ASRock Inc.		<b>Engineer:</b> Mars_Tseng	
Size A3	Project Name <b>G31M-VS2</b>	Rev 1.01	
Date: Tuesday, January 19, 2010		Sheet 16 of 36	



>>>MAA\_A[14..0] 5,16  
 >>>MBS\_A[2..0] 5,16  
 >>>MWE\_A# 5,16  
 >>>MCAS\_A# 5,16  
 >>>MRAS\_A# 5,16  
 >>>MCS\_A0# 5,16  
 >>>MCS\_A1# 5,16  
 >>>MODT\_A0 5,16  
 >>>MODT\_A1 5,16  
 >>>MCKE\_A0 5,16  
 >>>MCKE\_A1 5,16

1.00 DDR2 need termination signals :  
 CS#[3:0]  
 CKE[3:0]  
 ODT[3:0]  
 MA[13:0]  
 BS[2:0]  
 RAS#  
 CAS#  
 WE#

1.00 DDR2 Spec.  
 VDDQ 1.8V for DQ power  
 VDD 1.8V for power  
 VDDL 1.8V for DLL  
 power

G31M-VS2

<b>ASRock</b>		Title : <b>DDR2-CHA Power</b>	
ASRock Inc.		Engineer: <b>Mars_Tseng</b>	
Size <b>A3</b>	Project Name <b>G31M-VS2</b>	Rev <b>1.01</b>	
Date: <b>Tuesday, January 19, 2010</b>		Sheet <b>17</b> of <b>36</b>	

LF FootPrint

DDR2\_2A

MAA_B0	188	A0	DQ63	236	MD_B63
MAA_B1	183	A1	DQ62	235	MD_B62
MAA_B2	63	A2	DQ61	230	MD_B61
MAA_B3	182	A3	DQ60	229	MD_B60
MAA_B4	61	A4	DQ59	117	MD_B59
MAA_B5	60	A5	DQ58	116	MD_B58
MAA_B6	180	A6	DQ57	111	MD_B57
MAA_B7	58	A7	DQ56	110	MD_B56
MAA_B8	179	A8	DQ55	227	MD_B55
MAA_B9	177	A9	DQ54	226	MD_B54
MAA_B10	70	A10/AP	DQ53	218	MD_B52
MAA_B11	57	A11	DQ52	217	MD_B53
MAA_B12	176	A12	DQ51	108	MD_B51
MAA_B13	196	A13	DQ50	107	MD_B50
MAA_B14	174	A14	DQ49	99	MD_B48
	173	A15	DQ48	98	MD_B49
	×		DQ47	215	MD_B47
RCK_DIMM_B2	220	CK2P	DQ46	214	MD_B46
RCK_DIMM_B2#	221	CK2N	DQ45	209	MD_B45
RCK_DIMM_B1	137	CK1P	DQ44	208	MD_B44
RCK_DIMM_B1#	138	CK1N	DQ43	96	MD_B43
RCK_DIMM_B0	185	CK0P	DQ42	95	MD_B42
RCK_DIMM_B0#	186	CK0N	DQ41	90	MD_B41
MCS_B1#	76	CS1#	DQ40	89	MD_B40
MCS_B0#	193	CS0#	DQ39	205	MD_B38
MCKE_B1	171	CKE1	DQ38	200	MD_B37
MCKE_B0	52	CKE0	DQ37	199	MD_B36
			DQ36	87	MD_B35
			DQ35	86	MD_B39
MBS_B2	54	A16/BA2	DQ34	81	MD_B33
MBS_B1	190	BA1	DQ33	80	MD_B32
MBS_B0	71	BA0	DQ32	159	MD_B31
SMB_DATA_MAIN	119	SDA	DQ31	158	MD_B29
SMB_CLK_MAIN	120	SCL	DQ30	153	MD_B29
			DQ29	152	MD_B28
			DQ28	40	MD_B27
			DQ27	39	MD_B30
			DQ26	34	MD_B25
			DQ25	33	MD_B24
			DQ24	150	MD_B23
			DQ23	149	MD_B22
			DQ22	144	MD_B21
			DQ21	143	MD_B20
			DQ20	31	MD_B19
			DQ19	30	MD_B18
			DQ18	25	MD_B17
			DQ17	24	MD_B16
			DQ16	141	MD_B10
			DQ15	140	MD_B15
			DQ14	132	MD_B8
			DQ13	131	MD_B12
			DQ12	22	MD_B14
			DQ11	21	MD_B11
			DQ10	13	MD_B9
			DQ9	12	MD_B13
			DQ8	129	MD_B7
			DQ7	128	MD_B1
			DQ6	123	MD_B4
			DQ5	122	MD_B6
			DQ4	10	MD_B3
			DQ3	9	MD_B2
			DQ2	4	MD_B0
			DQ1	3	MD_B5
			DQ0		
				114	MDQS_B7
			DQS7P	113	MDQS_B7#
			DQS7N	105	MDQS_B6
			DQS6P	104	MDQS_B6#
			DQS6N	83	MDQS_B5
			DQS5P	82	MDQS_B5#
			DQS5N	84	MDQS_B4
			DQS4P	83	MDQS_B4#
			DQS4N	37	MDQS_B3
			DQS3P	36	MDQS_B3#
			DQS3N	28	MDQS_B2
			DQS2P	27	MDQS_B2#
			DQS2N	16	MDQS_B1
			DQS1P	15	MDQS_B1#
			DQS1N	7	MDQS_B0
			DQS0P	6	MDQS_B0#
			DQS0N		
				241	×
			NP_NC1	242	×
			NP_NC2	243	×
			NP_NC3	243	×

DDR\_DIMM\_240P

CK\_DIMM\_B2 RCK\_DIMM\_B2

CK\_DIMM\_B2# RCK\_DIMM\_B2#

CK\_DIMM\_B1 RCK\_DIMM\_B1

CK\_DIMM\_B1# RCK\_DIMM\_B1#

CK\_DIMM\_B0 RCK\_DIMM\_B0

CK\_DIMM\_B0# RCK\_DIMM\_B0#

MD\_B[63..0] 6  
MAA\_B[14..0] 6  
MBS\_B[2..0] 6  
MODT\_B[1..0] 6  
MDQM\_B[7..0] 6  
MCKE\_B[1..0] 6  
MCS\_B0# 6  
MCS\_B1# 6

MWE\_B# 6  
MCAS\_B# 6  
MRAS\_B# 6

CK\_DIMM\_B0 6  
CK\_DIMM\_B0# 6  
CK\_DIMM\_B1 6  
CK\_DIMM\_B1# 6  
CK\_DIMM\_B2 6  
CK\_DIMM\_B2# 6

MDQS\_B7# 6  
MDQS\_B7 6  
MDQS\_B6# 6  
MDQS\_B6 6  
MDQS\_B5# 6  
MDQS\_B5 6  
MDQS\_B4# 6  
MDQS\_B4 6  
MDQS\_B3# 6  
MDQS\_B3 6  
MDQS\_B2# 6  
MDQS\_B2 6  
MDQS\_B1# 6  
MDQS\_B1 6  
MDQS\_B0# 6  
MDQS\_B0 6

SMB\_CLK\_MAIN 12,15,16  
SMB\_DATA\_MAIN 12,15,16

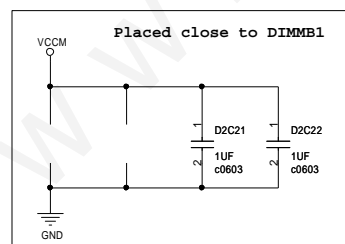
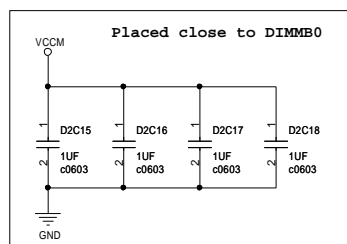
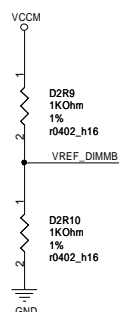
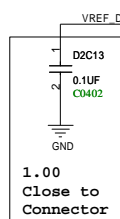
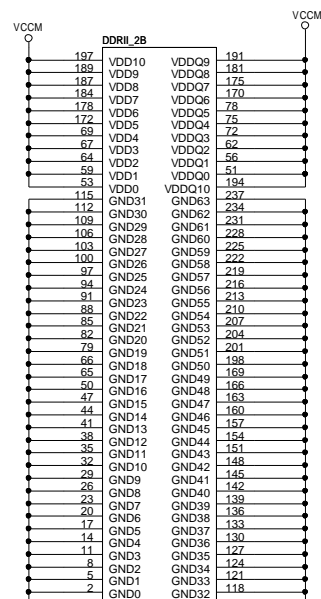
G31M-VS2

<b>ASRock</b>		<b>Title : DDR2-CHB Control</b>	
ASRock Inc.		Engineer: Mars_Tseng	
Size	Project Name	Rev	
A3	G31M-VS2	1.01	
Date: Tuesday, January 19, 2010		Sheet 18 of 36	

1.00 DDR2 need termination signals :

CS#[3:0]  
 CKE[3:0]  
 ODT[3:0]  
 MA[13:0]  
 BS[2:0]  
 RAS#  
 CAS#  
 WE#

MAA\_B[14..0] 6,18  
 MBS\_B[2..0] 6,18  
 MWE\_B# 6,18  
 MCAS\_B# 6,18  
 MRAS\_B# 6,18  
 MCS\_B0# 6,18  
 MODT\_B0 6,18  
 MCS\_B1# 6,18  
 MODT\_B1 6,18  
 MCKE\_B0 6,18  
 MCKE\_B1 6,18

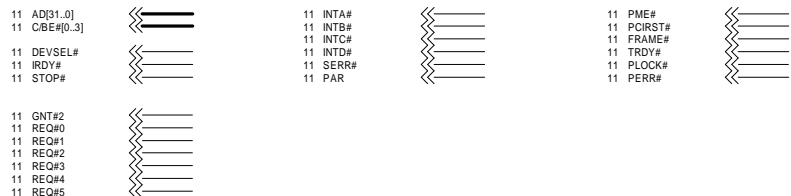


G31M-VS2

<b>ASRock</b>		<b>Title : DDR2-CHB Power</b>	
ASRock Inc.		Engineer: Mars_Tseng	
Size A3	Project Name G31M-VS2	Rev 1.01	
Date: Tuesday, January 19, 2010		Sheet 19 of 36	

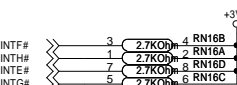
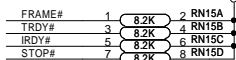
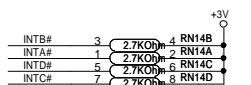
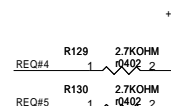
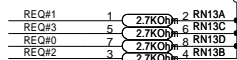
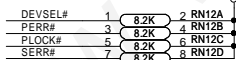
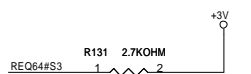
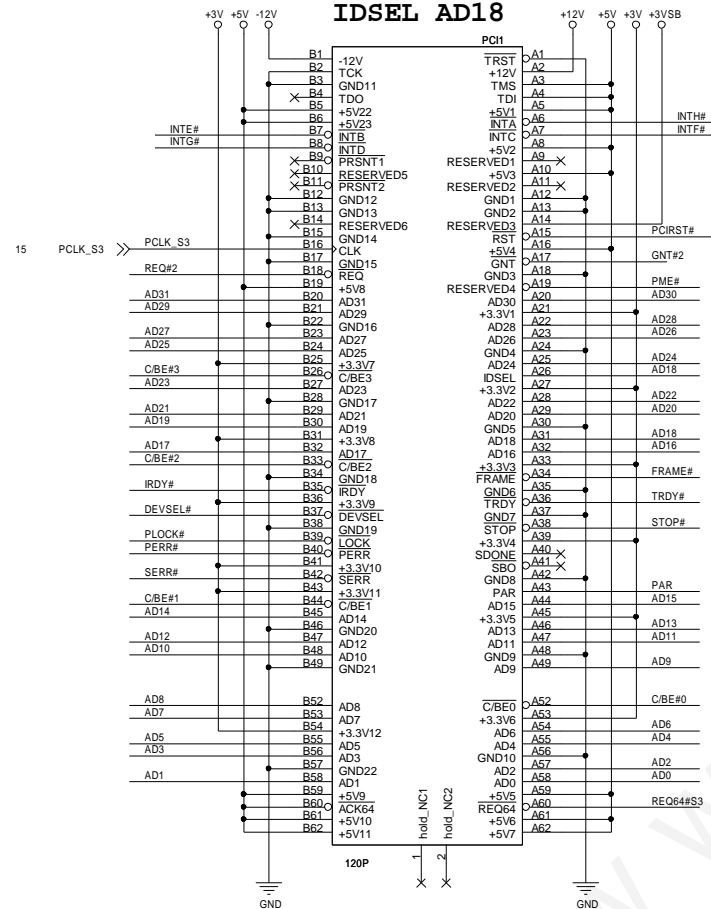






## PCI SLOT1

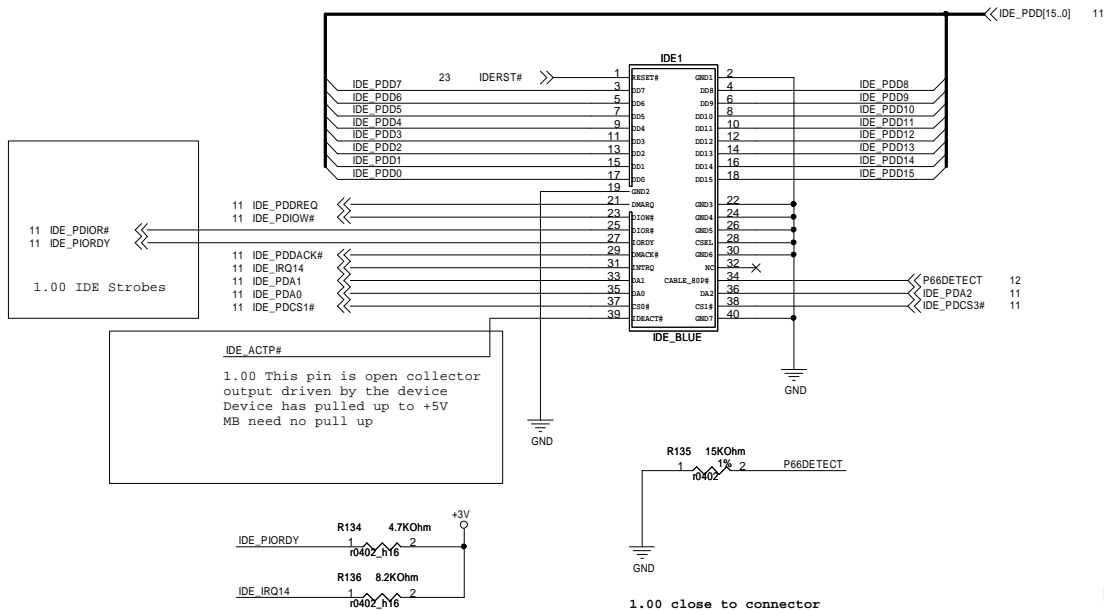
### HEFG IDSEL AD18



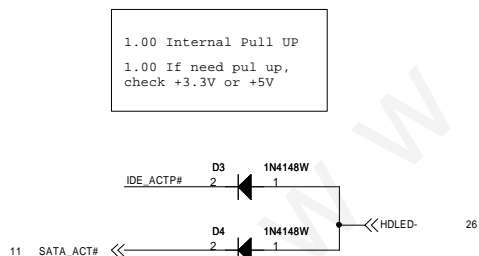
G31M-VS2

<b>ASRock</b>		Title : PCI SLOT	
ASRock Inc.		Engineer: Mars_Tseng	
Size A3	Project Name G31M-VS2	Rev 1.01	
Date: Tuesday, January 19, 2010		Sheet 21 of 36	

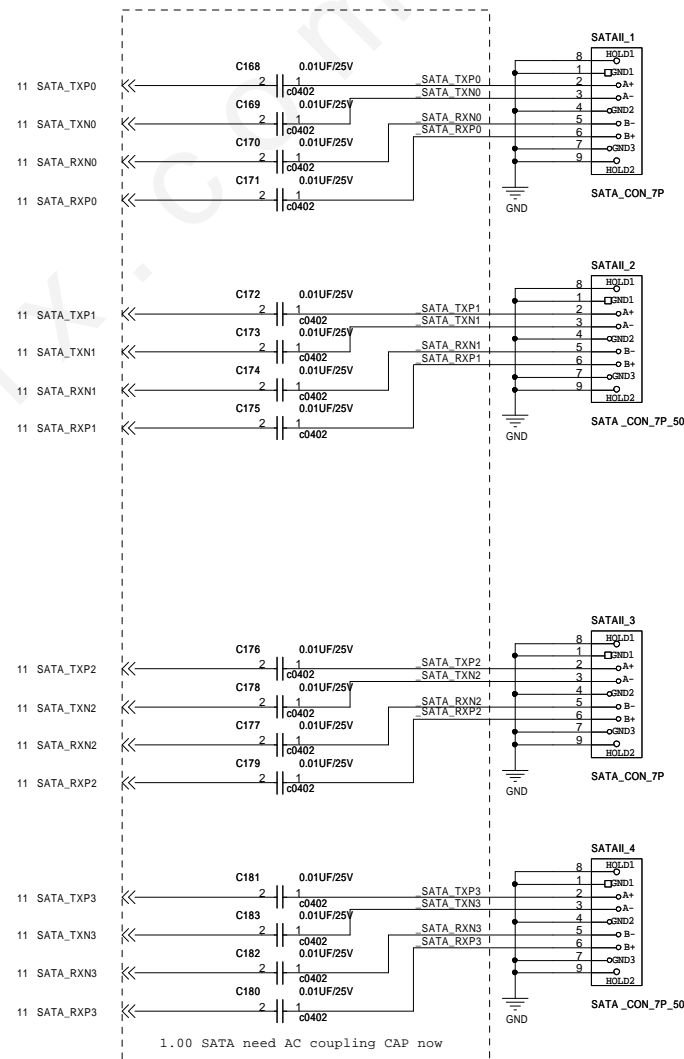
**IDE**



## IDE & SATA LED



## Serial ATA

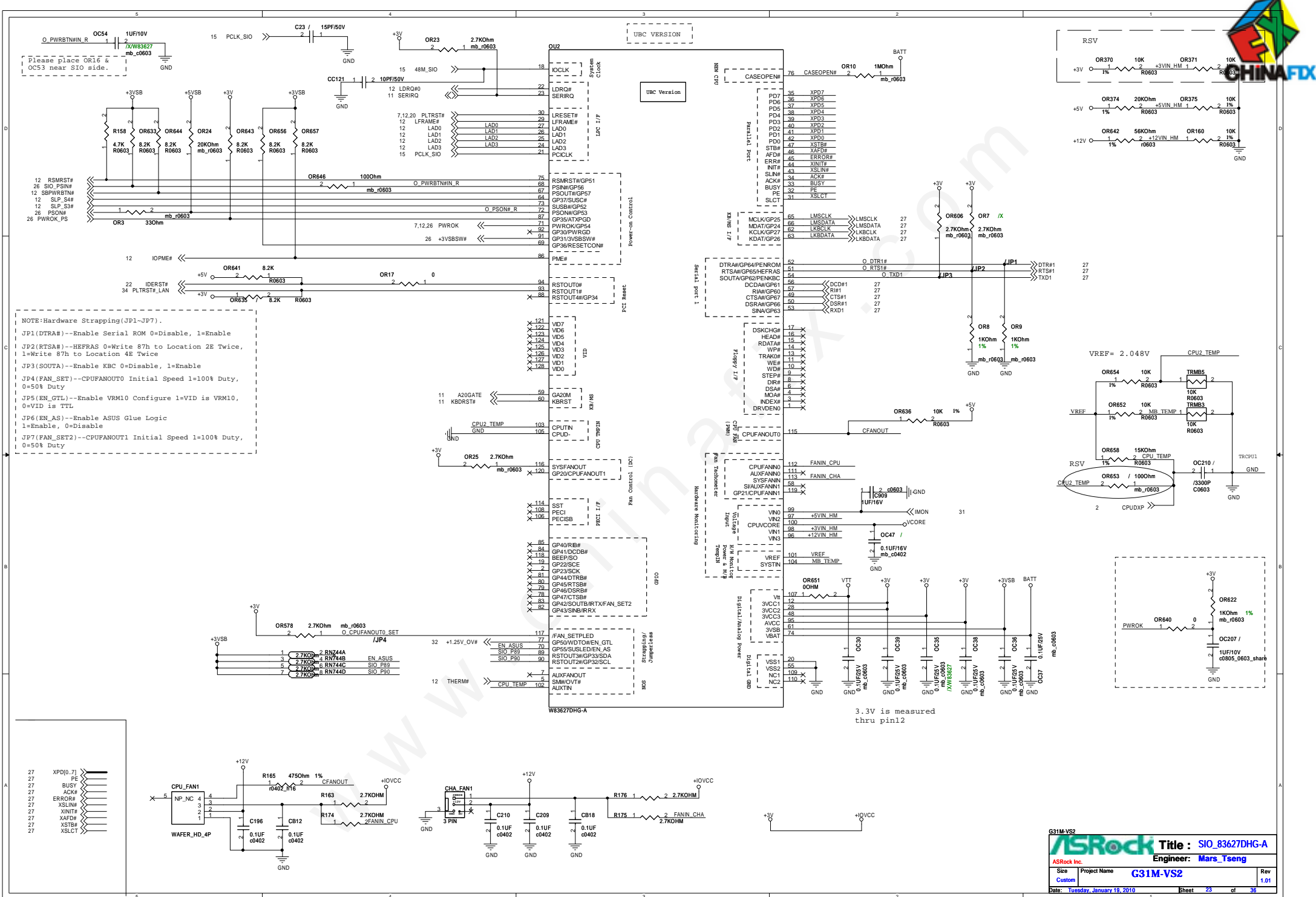


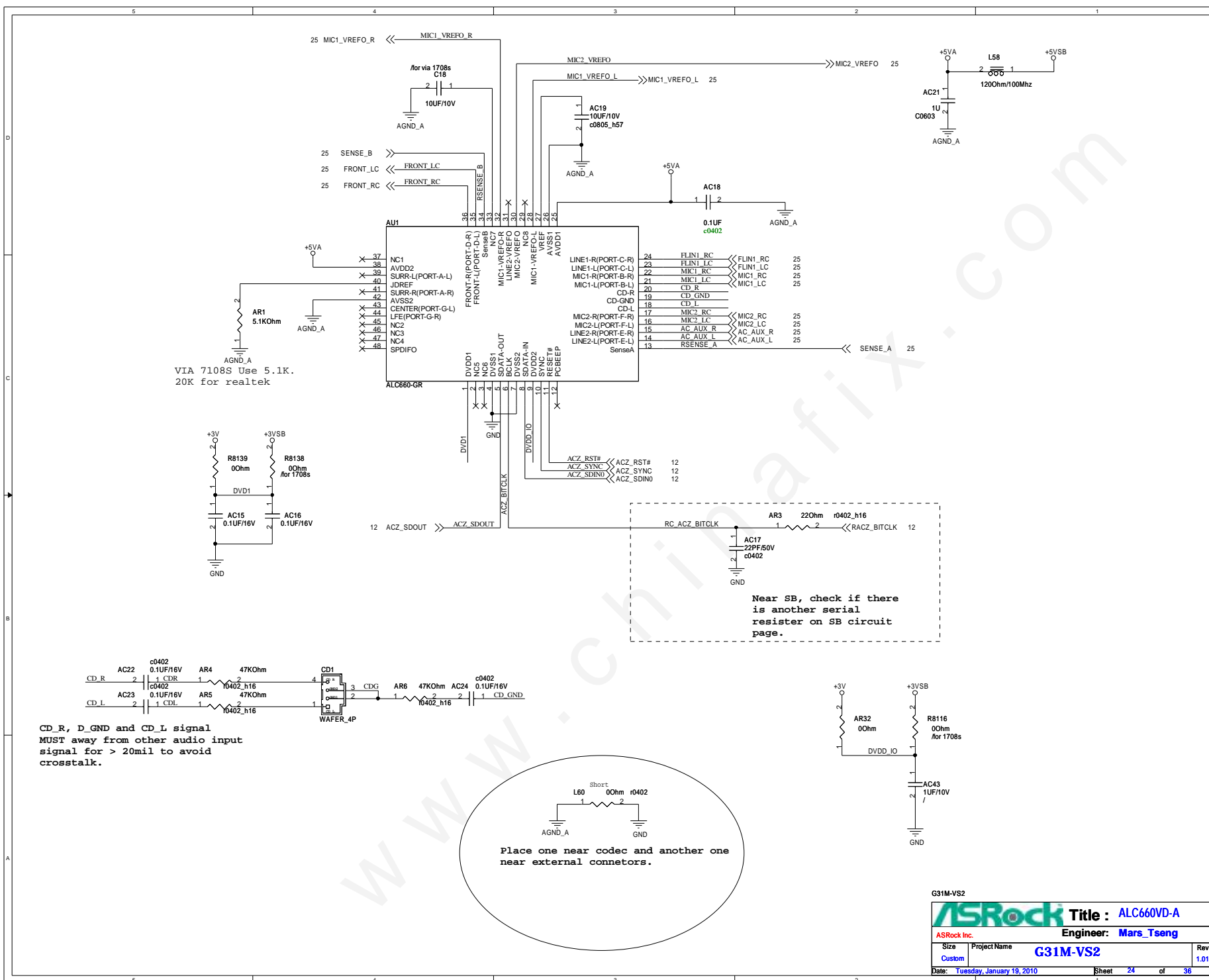
1.00 AC coupling CAP must  
minimize the placement mismatch  
G31M-VS2 within a differential pair.

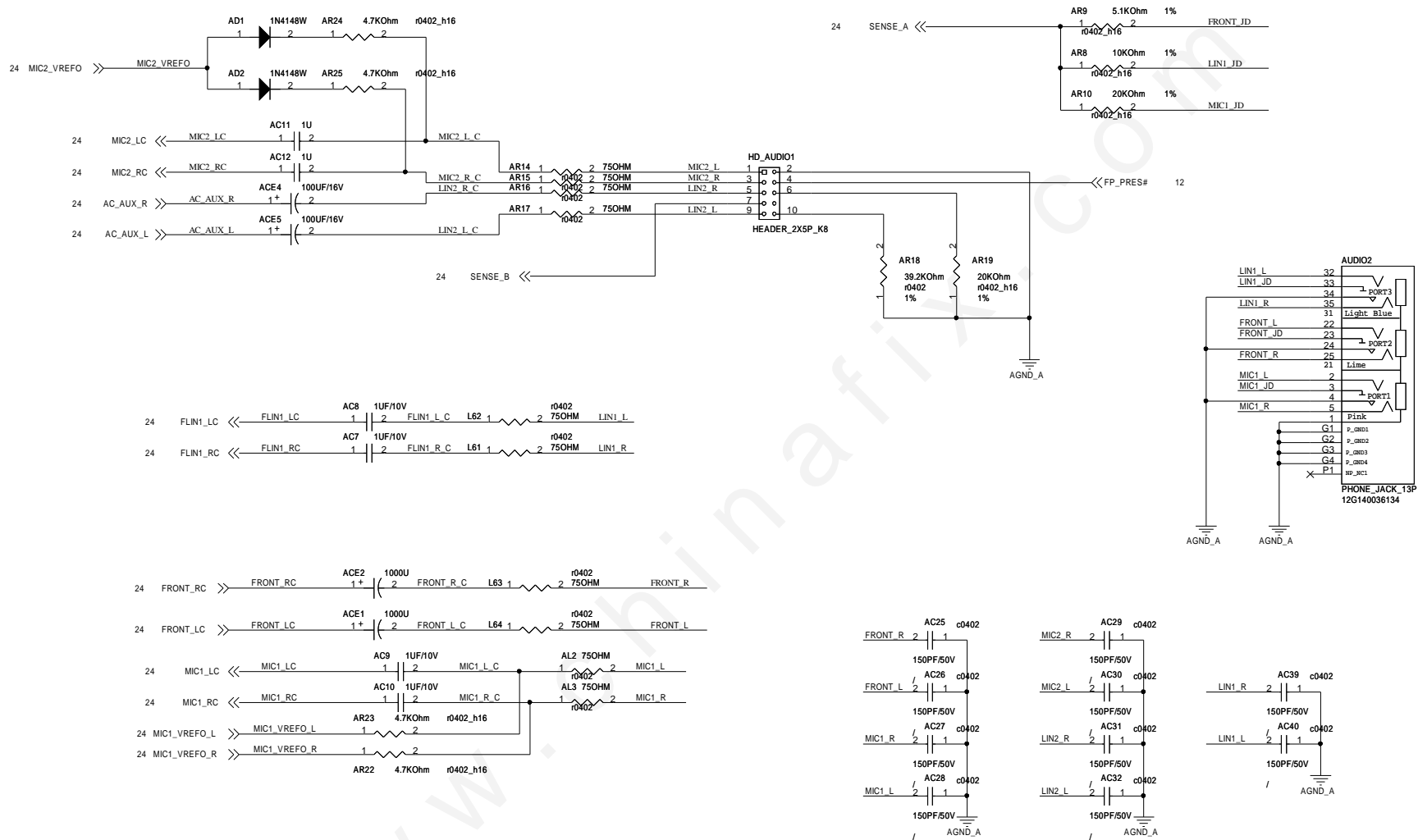
ASRock Title : IDE & SATA

ASRock Inc. Engineer: Mars\_Tseng

Size <b>A3</b>	Project Name <b>G31M-VS2</b>	Rev <b>1.01</b>
Date: <b>Tuesday, January 19, 2010</b>		Sheet <b>22</b> of <b>36</b>



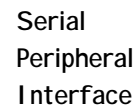






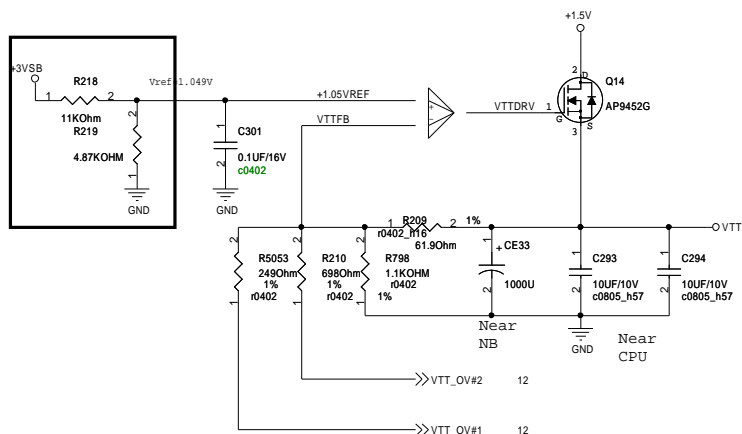




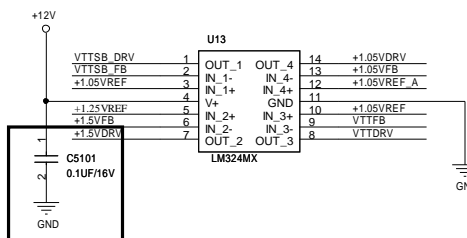


PDF created with pdfFactory trial version [www.pdffactory.com](http://www.pdffactory.com)

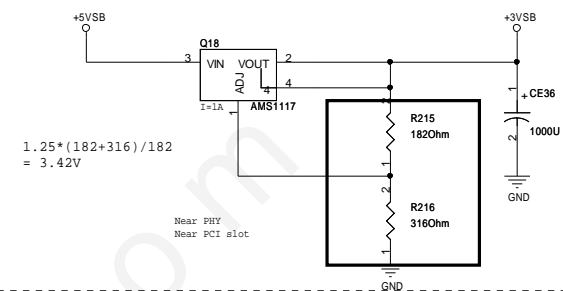
### +1.5V to VTT



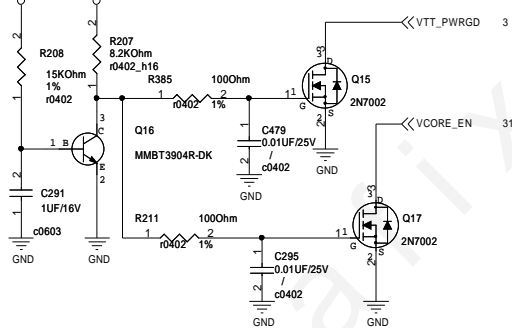
### LM324



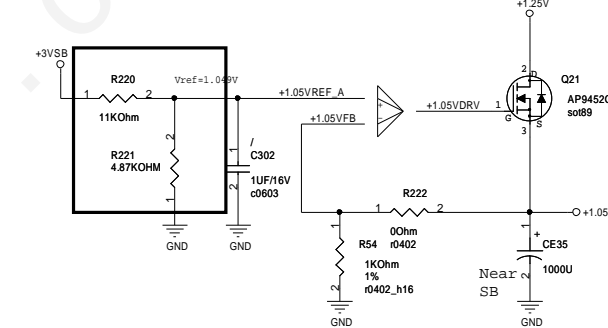
### +5VSB to +3VSB



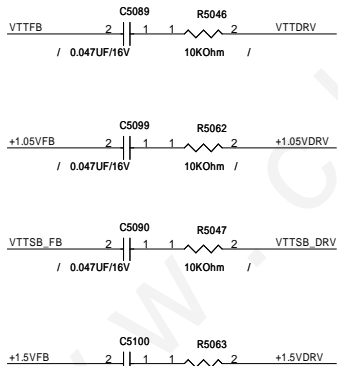
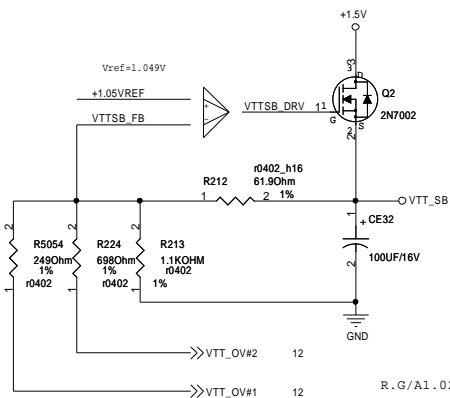
### Vcore Enable Function



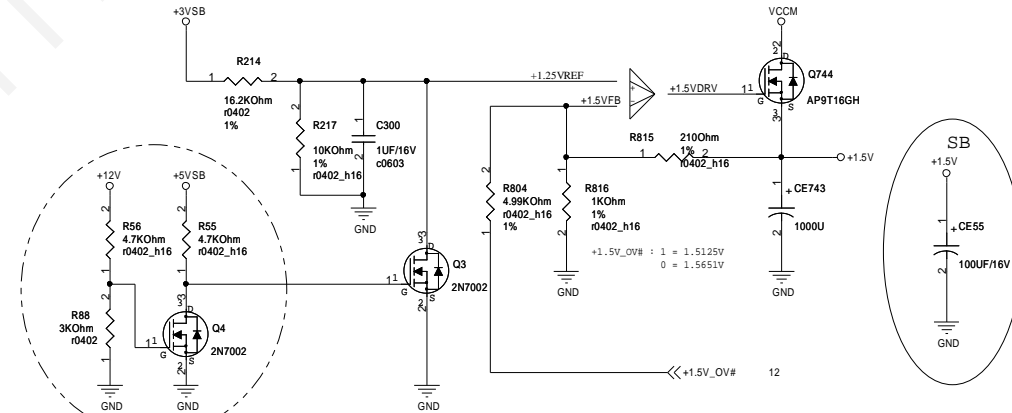
### +1.25V to +1.05V



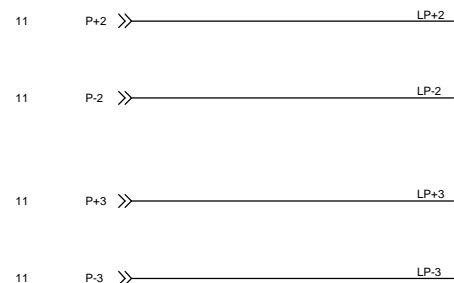
### +1.5V to VTT\_SB



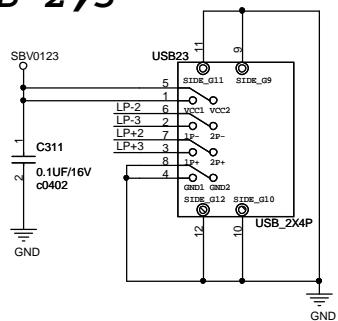
### VCCM to +1.5V



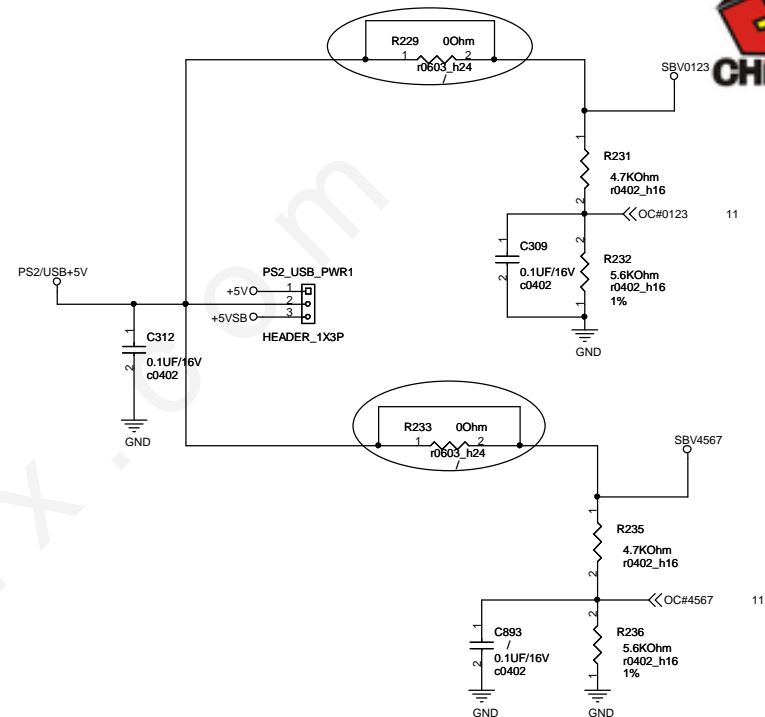
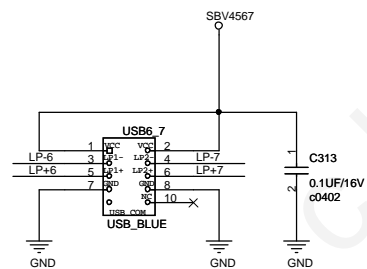
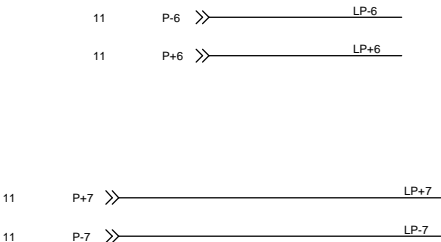
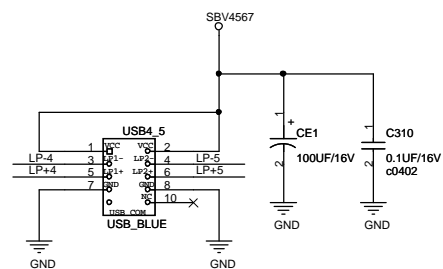
S3 Function circuit (when S3, +1.5V become to +0V)



## USB 2,3



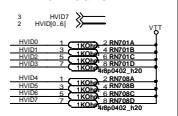
## USB 4,5



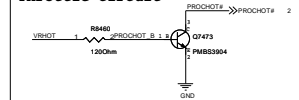
G31M-VS2

<b>ASRock</b>		<b>Title : USB PORT</b>	
ASRock Inc.		Engineer: Mars Tseng	
Size	Project Name	G31M-VS2	Rev
Custom			1.01
Date: Tuesday, January 19, 2010		Sheet	30 of 36

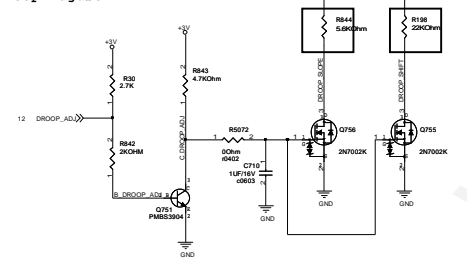
# VID circuit



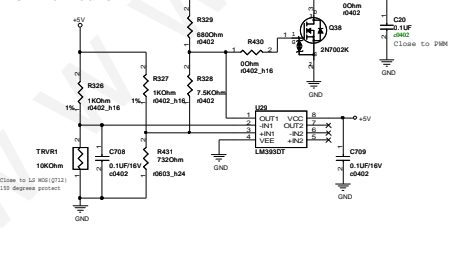
# Throttle circuit



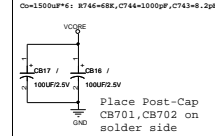
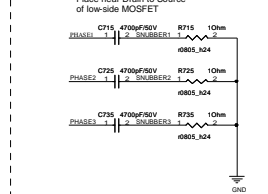
# Drop Adjust

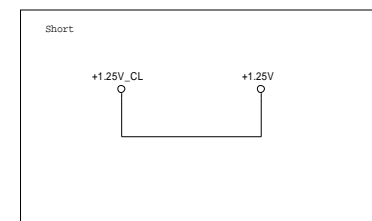
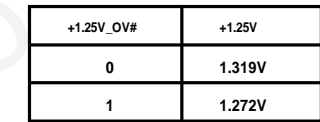


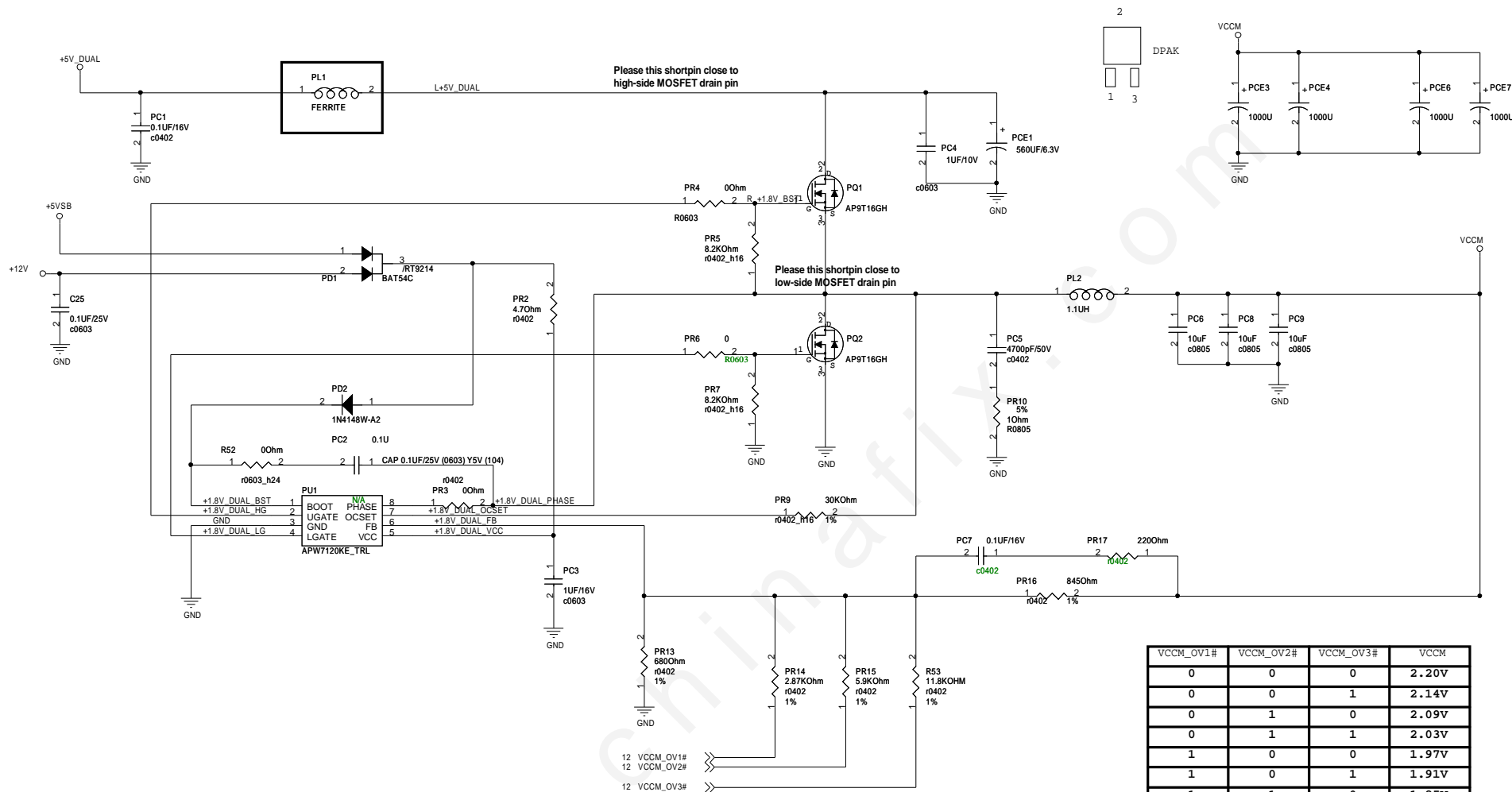
# OTP circuit



# Snubber Circuit







G31M-VS2

<b>ASRock</b>		Title : +1.8V_Dual	
ASRock Inc.		Engineer: Mars_Tseng	
Size	Project Name	G31M-VS2	
Custom			Rev 1.01
Date: Tuesday, January 18, 2010		Sheet 33	of 36



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